

U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.		Serial No.	
						M-11822 US		09/925,102	
<div style="border: 1px solid black; border-radius: 50%; padding: 10px; display: inline-block;"> INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) JUL 27 2002 PATENT & TRADEMARK OFFICE </div>						Applicant(s)			
						Jack H. Yuan et al.			
						Filing Date		Group	
						August 8, 2001		2185	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
PD	AA	5,043,940	Aug. 27, 1991	Harari			<div style="text-align: right;"> RECEIVED JUL 30 2002 Technology Center 2100 </div>		
	AB	5,070,032	Dec. 3, 1991	Yuan et al.					
	AC	5,095,344	Mar. 10, 1992	Harari					
	AD	5,172,338	Dec. 15, 1992	Mehrotra et al.					
	AE	5,297,148	Mar. 22, 1994	Harari et al.					
	AF	5,313,421	May 17, 1994	Guterman et al.					
	AG	5,315,541	May 24, 1994	Harari et al.					
	AH	5,343,063	Aug. 30, 1994	Yuan et al.					
	AI	5,661,053	Aug. 26, 1997	Yuan					
	AJ	5,712,180	Jan. 27, 1998	Guterman et al.					
PD	AK	6,103,573	Aug. 15, 2000	Harari et al.					
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
PD	AL	Aritome, Seiichi, "Advanced Flash Memory Technology and Trends for File Storage Application," IEDM Technical Digest, International Electronic Devices Meeting, IEEE, San Francisco, California, December 10-13, 2000, pp 33.1.1-33.1.4.							
	AM	Takeuchi, Y., et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable 1Gbit Flash Memories," 1998 Symposium on VLSI Technology; Digest of Technical Papers, IEEE, Honolulu, Hawaii, June 9-11, 1998, pp. 102-103.							
	AN	Lee, Jae-Duk, et al., "Effects of Parasitic Capacitance on NAND Flash Memory Cell Operation," Non-Volatile Semiconductor Memory Workshop, IEEE, Monterey, California, August 12-16, 2001, pp. 90-92.							
PD	AO	Chan, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," <i>IEEE Electron Device Letters</i> , Vol. EDL-8, No. 3, March 1987, pp. 93-95.							
Examiner		PHUC T. DANG		Date Considered		2/26/04			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.		
				M-11822 US		09/925,102		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)		RECEIVED		
(Use several sheets if necessary)				Jack H. Yuan et al.		JUL 30 2002		
				Filing Date		Group		
				August 8, 2001		Technology Center 2100 2185		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
PD	AP	6,151,248	Nov. 21, 2000	Harari et al.				
PD	AQ	6,222,762	Apr. 24, 2001	Guterman et al.				
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
PD	AR	Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," <i>IEEE Journal of Solid State Circuits</i> , Vol. 26, No. 4, April 1991, pp. 497-501.						
	AS	Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 11, November 2000, pp. 543-545.						
	AT	DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO ₂ injectors and a floating polycrystalline silicon storage layer," <i>J. Appl. Phys.</i> 52(7), July 1981, pp. 4825-4842.						
PD	AU	Hori et al., "A MOSFET with Si-implanted Gate-SiO ₂ Insulator for Nonvolatile Memory Applications," <i>IEDM 92</i> , April 1992, pp. 469-472.						
Examiner		PAUC T. DANG		Date Considered		2/26/04		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

U.S. Department of Commerce, Patent and Trademark				Atty. Docket No.		Application No.		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				SNDK.257US0		09/925,102		
(Use several sheets if necessary)				Applicant(s)				
				Jack H. Yuan et al.				
				Filing Date		Group		
				Aug. 8, 2001		2818		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
PD	AA	5,963,889	10/05/1999	Yamauchi				
PD	AB	6,048,768	04/11/2000	Ding				
PD	AC	6,103,573	08/15/2000	Harari				
PD	AD	6,509,222	01/21/2003	Grossi				
PD	AE	6,518,618	02/11/2003	Fazio				
U.S. Published Patent Application Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
PD	AF	02/25025	07/08/2002	Intl. Search Report				
Foreign Patent Documents								
		Document	Date	Country	Class	Subclass	Translation	
							Yes	No
PD	AG	WO 01/41199	07.06.2001	PCT				
PD	AH	EP 0 780 902 A1	25.06.1997	EP				
PD	AI	EP 1 104 023 A1	30.05.2001	EP				
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
Examiner	PHUZ T. DANG		Date Considered		2/26/04			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								